Subject: PCIe-AS - What are limitations on Network size ?
Posted by Walter F.J. Müller on Tue, 14 Sep 2004 13:47:49 GMT
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During E. Denes talk on the 2nd FutureDAQ workshop the question was raised what the size limit of AS networks is.

In several places I found statements to the effect that the design goal for PCIe-AS was to support 'small' networks with a size of 1000 or 10000 nodes.

The turn pool size is 31 bits (see previous post). Each switch only requires as many bits in the turn pool as is needed to enumerate his ports. This allows to express a path through 10 8-port switches, or through 7 16-port switches, or through 6 32-port switches, more than enough to handle 1000 to 10000 end nodes.

The PNet based on 3 cascaded 8-port switches shown in my talk needes only a 9 bit path address. The BNet can in principle be build from two layers of 24-port swiches, so needs only 10 bit path addresses. So I assume, that even a combined BNet/PNet would not challenge the 31 bit path address length limit of PCIe-AS.

{16.9.2000: fixed DocuMana link which had changed...}

Subject: Re: PCIe-AS - What are limitations on Network size ?
Posted by Walter F.J. Müller on Wed, 15 Sep 2004 09:10:03 GMT
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Walter F.J. Müller wrote on Tue, 14 September 2004 15:47The PNet based on 3 cascaded 8-port switches shown in my talk needes only a 9 bit path address.

This isn't correct. Since 4 8-port switches have to be traversed, see the attached figure, one needs 4*3 = 12 bits.

At this place another correction: In my talk I mistakenly wrote that the PEX 8532 is a AS switch. It is a PCIe switch, a true AS switch is announced.

File Attachments

1) 4switch.png, downloaded 1174 times