Subject: LYCCA - w-DSSSD Time Gated
Posted by thuyuk on Wed, 13 Aug 2014 10:48:08 GMT
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Hi all,

I would like to make use of LYCCA.DSSDTimeGated processor but I have some information missing: I couldn't locate the time signals of the p-side of the silicons in Crates.config. Would you be so kind to help me to update my config files?

Thank you very much in advance!

Tayfun

Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by miree on Wed, 13 Aug 2014 12:01:29 GMT
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Here is the layout of the Target and ToF crate as it was used in the 2014 campaign. I believe it was the same in 2012

```
crate  LyccaTargetTofCrate
   procid   90
   module   adc0    LYCCA.v785      # Target DSSSD p-side amplitudes
   module   adc1    LYCCA.v785      # Target DSSSD n-side amplitudes
   module   tdc     LYCCA.v775      # Target DSSSD times (I don't know if p- or n-side times)
   module   mhtdc0  LYCCA.v1290TMM  # ToF scintillators
   module   mhtdc1  LYCCA.v1290TMM  # ToF scintillators
   module   mhtdc2  LYCCA.v1290TMM  # ToF scintillators
end
```

Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by thuyuk on Wed, 13 Aug 2014 12:06:40 GMT
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Hi Michael,

Thank you very much for your reply.

I seems that I have the same layout. I'm a little bit confused: Do we have the time signals from one of the sides of the wall-DSSSD detectors?

Thank you!

Subject: Re: LYCCA - w-DSSSD Time Gated

Posted by miree on Wed, 13 Aug 2014 12:27:05 GMT
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Hi,

yes... the TargetDSSSD times where not always present in the 2014 campaign . I don't remember if there were similar problems in 2012. It could be that this module didn't read the TargetDSSSD time signals.
Here are the WallDSSSD unpackers. The Wall DSSSD times are read by the CAENv767 multihit TDCs. They have 128 channels, which is enough for one side of all DSSSD modules in each crate. Again I'm not sure if p- or n-side times are read. As far as I remember, these were always present.

While analyzing commissioning data, I never used these time signals. Perhaps someone in the LYCCA collaboration has experience in how this information can be used.


```
crate LyccaWallCrate1
  procid   70
  module   adc01   LYCCA.v785
  module   adc02   LYCCA.v785
  module   adc05   LYCCA.v785
  module   adc06   LYCCA.v785
  module   adc07   LYCCA.v785
  module   adc08   LYCCA.v785
  module   adc11   LYCCA.v785
  module   adc12   LYCCA.v785
  module   mhtdc   LYCCA.v767
end

crate LyccaWallCrate2
  procid   80
  module   adc13   LYCCA.v785
  module   adc14   LYCCA.v785
  module   adc17   LYCCA.v785
  module   adc18   LYCCA.v785
  module   adc19   LYCCA.v785
  module   adc20   LYCCA.v785
  module   adc23   LYCCA.v785
  module   adc24   LYCCA.v785
  module   mhtdc   LYCCA.v767
end
```


Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by thuyuk on Wed, 13 Aug 2014 12:30:36 GMT
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All right! Thanks a lot for the crate entries for the time signals of w-DSSSD!

Cheers,

Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by Damian Ralet on Wed, 13 Aug 2014 12:33:47 GMT

Hi Tayfun,

I did not look at it myself, but I know that Pico was looking at the timing of the target DSSD, and he was having time information for the Pb experiment.
He presented a few slides on his anlysis during the EGAN meeting this year.

Cheers,
Damian

Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by thuyuk on Wed, 13 Aug 2014 12:37:49 GMT

Hi Damian,

Thanks a lot for the information.

I made use of the time of Target-DSSSD, but my intention was to make use of the Wall-DSSSD. We are suspecting possible pile-ups due to the high counting rate. We thought it might be useful to use a condition on time of the detector itself to suppress artificial effects. Maybe we are wrong but we would like to try it anyway

Cheers

Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by mlcortes on Wed, 13 Aug 2014 13:24:00 GMT

Hi Tayfun,

We looked at the times of the WallDssd for the Pb data of 2012. As Michael mentioned, the times of the wall (only the p-side) are read by Multihit modules. What we did, and seems to work quite fine, is to select the first hit of this modules and use it as the input for the Dssd processor. By doing this I can see nice time-energy spectra for all the modules. This selection (for my data) removes the need of a time-energy gate, so you can keep using the normal DSSD processor. I think there you can see if you need an aditional gate for your case
Actually we see a double time structure that seems to come from the diferent electronic chain of the modules 19,20,23 and 24. If you see the same, let us know! We are still not sure about the origin of it.
The code I am using goes like this:
Before the DSSD processors I select the hit

```
processor Lycca/WallDssdPreproc  UTILS.HitPick
   input_array[0:127]  <-  LyccaWallCrate1.tdc[0:127]
```

```
#   display out_first
end
processor Lycca/WallDssdPreproc1  UTILS.HitPick
  input_array[0:127]  <-  LyccaWallCrate2.tdc[0:127]
#   display out_first
end
```

And after that I put the time input if the DSDD processor. Here i copy just an example of the module 01 with all the inputs and visualization

```
processor Lycca/WallDssd01 LYCCA.DSSSD
   #triggers 8 9 10
 amplitude_p[0:15]  <-  LyccaWallCrate1.adc01[0:15]
 amplitude_n[0:15]  <-  LyccaWallCrate1.adc01[16:31]
 time_p[0:15] <- Lycca/WallDssdPreproc.out_first[0:15]
 display time_p        in WallDssd/Module01/time_p
    display amplitude_p 2048,0,4096         in WallDssd/Module01/amplitude_p
    display amplitude_n 2048,0,4096         in WallDssd/Module01/amplitude_n
    display multiplicity_p 32,0,32        in WallDssd/Module01/multiplicity
    display multiplicity_n 32,0,32        in WallDssd/Module01/multiplicity
  display multiplicity_t 32,0,32     in WallDssd/Module01/multiplicity
 display multiplicity_p:multiplicity_t     in WallDssd/Module01/multiplicity 32,0,32: 32,0,32
 display cluster_multiplicity_p 32,0,32    in WallDssd/Module01/cluster_multiplicity
    display cluster_multiplicity_n 32,0,32    in WallDssd/Module01/cluster_multiplicity
    display cal_amplitude_p:cal_amplitude_n    in WallDssd/Module01
    display amplitude_p:amplitude_n        in WallDssd/Module01
    display dE                in WallDssd/Module01
   display cal_time_p        in WallDssd/Module01/cal_times
 display cal_time_p:cal_amplitude_p    in WallDssd/Module01
 display time_p_sum:dE_p  500,0,10000:500,300,4000  in WallDssd/Module01
end
```

The last spectra should show you a nice energy time plot. Hope this is useful for you and let us know if you have any problem

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Subject: Re: LYCCA - w-DSSSD Time Gated
Posted by thuyuk on Wed, 13 Aug 2014 16:57:04 GMT
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Hi Liliana,

Many thanks for sharing the related part of the config file.

One question: In the DSSD module 12, the cable assignment doesn't follow the trend, e.g.:

```
 amplitude_p[0:13]  <-  LyccaWallCrate1.adc12[0:13]
```

amplitude_p[15] <- LyccaWallCrate1.adc12[15]
amplitude_n[0:15] <- LyccaWallCrate1.adc12[16:31]

do you know if the same applies for the time signals?

Thanks!
Tayfun

edit: Sorry! I just saw that only strip #14 is missing. I certainly can handle this! Please ignore this message.