The Time Distribution System

I. Introduction.

Timing and synchronization are common problems of high rate experiments in the field of particle physics. In order to synchronize the data and provide a time reference for high precision timing measurements the Time Distribution System (*TDS*) is needed. The system provides an absolute time by distributing the reference clock down to the level of the frontend electronics, i.e. very close to the detectors. The frontend electronics measures the timing of the detector signal respectively to the clock, adds an absolute time stamp and sends this information to the next level of the DAQ.

II. Requirements.

- The maximum jitter of the time reference is 20 ps.
- The system is scalable from few hundred to few thousand destinations.
- The components of the TDS can be mounted on the frontend modules very close to the detectors where radiation conditions exceed normal radiation level, therefore the components should be radiation tolerant.
- The time distribution system is flexible in order to follow the development and new requirements of the experiment.

III. Architecture.

The architecture of the proposed Time Distribution System is based on existing systems like the TTC for LHC experiments [1], and the TCS [2] [3], built for the COMPASS experiment at CERN [4]. The precise time reference is provided by distributing an encoded clock and data from a single source via a passive optical network to a large number of destinations. The basic architecture of the TDS is shown in figure 1 and includes only unidirectional data transfer, but we plan to study the possibility of using the existing optical network with a bidirectional interface. The bidirectional network will allow to combine the functionality of the time distribution system with the frontend interface. We are considering to exploit one of two possible methods to implement the bidirectional network using the TDS architecture:

- use passive splitters as a concentrator for transferring the light signals from all destinations to the central Master module. This is possible because the light splitter has an asymmetric attenuation parameters depending on the light propagation direction. The disadvantage of this method is that only one TDS receiver can power the laser diode and switching from TDS receiver to another one takes significant amount of time due to resynchronization of the SerDes at the TDS master module.
- use active concentrators which combine information from 32 sources to one destination. This solution is certainly feasible but the reliability of the system has to be evaluated.

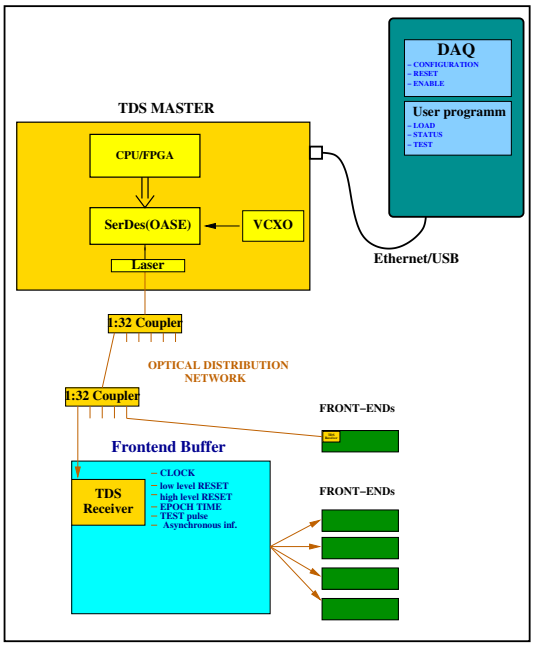

Fig. 1. The TDS system, functional diagram

The Time Distribution System includes three main components:

- TDS master module with integrated laser transmitters;
- passive optical network with 1:32 splitters;
- TDS receivers.

The TDS master module is a central module of the system which includes:

- the processor or/and an FPGA to control the system;
- the temperature compensated crystal oscillator,
- OASE serializer/deserializer chip,
- the interface to the control software, DAQ and user programms;
- the control signal inputs,
- input/outputs for extending the system to a bigger number of destinations.

The TDS receiver is a small mezzanine card with the OASE chip and the FPGA. The pin and laser diodes are integrated into the SerDes chip. The FPGA receives data from the SerDes chip, extracts control signals and provides asynchronous information to the destination module via serial link. Every TDS receiver has its own unique ID for addressing and configuration the receiver via the optical link.

IV. Clock and data Encoding.

The clock and data are encoded in a single serial line by using standard 8 bit / 10 bit encoder. Using a serializer/deserializer(SerDes) at a high speed of 2 Gbit/s, which becomes a standard in these days, will eliminate the problem of clock jitter.

The most suitable candidate for the SerDes chip is the OASE chip which is being developed by the University of Mannheim in cooperation with the company ULM Photonics (Ulm). The functional diagram of the chip is shown in figure 2.

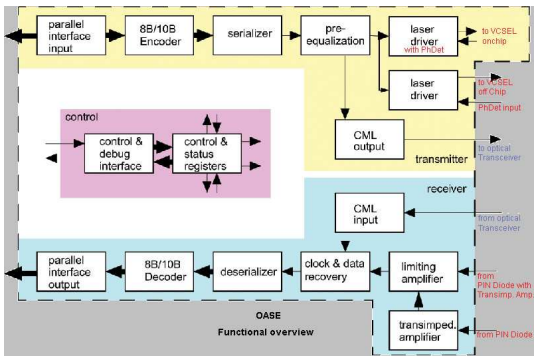

Fig. 2. OASE chip, functional diagram

The development of the OASE chip is a part of the FutureDAQ project and gives a possibility to implement features which are specific for the time distribution system:
- radiation tolerant behaviour of digital electronics by designing the state machines and data transfer interfaces with a single bit error recovery logic;
- clock phase adjustment to compensate the fibre length and the position of the detector respectively to the target;
- clock divider to provide the front-ends with desired clock frequency;

The phase adjustment can be done with a precision of the serial data clock period i.e. if the SerDes transmits data with 2.5 Gbit/sec then the clock phase can be adjusted with the precision of 400ps.
The parallel interface of the SerDes chip at the TDS receiver side is synchronized to 1/10 of the serial data clock i.e. 250MHz. Most of the front-end modules expected to use lower frequency for clocking TDC, ADC chips and processing logic there for the SerDes chip provides any other frequency which can be obtained by deviding the 250 MHz clock. The division coefficient is an integer number and programmed via the TDS master module and the phase of the clock is defined by the low and high level RESET signals.

V. Synchronous and asynchronous information.

The TDS distributes two classes of information: synchronous and asynchronous. The synchronous information is a time critical control information, which is distributed with fixed latency. The synchronous information is decoded at the destination and provided as control signals to the front-end modules.

The synchronous information or control signals:
- low level RESET - reloads FPGAs, resynchronizes PLL and DLL ;
- high level RESET - resets all data buffers, counters and state machines, it also defines the TIME ZERO in the experiment;
- GLOBAL ENABLE - enables/disables data taking in all front-ends ;
- EPOCH TIME - the signal is distributed with a fixed time interval, generates the EPOCH TIME information on the data stream and allows to verify the synchronization of the destination module;
- TEST PULSE - initiate generation of the test pattern on the data stream, the test patterns allow to verify the integrity of the FE-DAQ interfaces.

The asynchronous information is distributed for configuration of the TDS receivers.

References

[1] http://ttc.web.cern.ch/TTC/intro.html

[2] I.Konorov et al.. The trigger control system for the COMPASS Experiment. In IEEE Nuclear Science Symposium Conference Record (2002).

[3] L.Schmitt et al.. The DAQ of the COMPASS Experiment. IEEE Trans. Nucl. Sci.(2004).

[4] http://wwwcompass.cern.ch